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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,466	10/17/2005	Kazuhiro Kondo	274621US6PCT	8941
22850	7590	11/30/2006	EXAMINER	
C. IRVIN MCCLELLAND OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			CRANE, SARA W	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/553,466

Applicant(s)

KONDO, KAZUHIRO

Examiner

Sara W. Crane

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japan 05-109977, in view of Yoshida et al. and Mimura et al.

With respect to claim 1, figures 3 and 4 of 05-109977 show a first and second chip, where the larger chip at the bottom has an electrode pattern at the edge connected to wiring 4, for an external connection. There is a second electrode portion at 2 for connecting to a circuit in the second or top chip. There is a third electrode pattern in the shape of a square for connecting to a block-shaped circuit in the top chip. The top or second chip has a fourth electrode portion at 5 for connecting to the second electrode portion in the lower chip, and a fifth electrode portion in the shape of a square for connecting to the third electrode portion in the lower chip. The specific micro-bump bonding is taught at Yoshida et al. column 8, lines 64-65, where figure 9 shows two matching bumps 4a and 4b, one on a top chip, and the other on the bottom chip, for making the contact. Mimura et al. notes in addition at column 12, 45-50, that micro bump bonding has the advantage of very small pitches. It would have been obvious to provide a set of micro bumps at the contact areas on each of the top and the bottom

chips of the Japan reference, as taught with respect to figure 9 of Yoshida et al., for the reason taught by Mimura et al.

With respect to claim 2, it would have been obvious to arrange the mating top and bottom squares of electrodes of the Japan reference in the middle of the chips, as taught by figure 12 of Mimura et al., in order to optimize layout as shown with respect to the circuits of this reference. It would have been obvious to arrange the external contacts in the peripheral portion of the chips, because, if the square is in the middle, the peripheral portions would be the areas that are free for the other contacts.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references discussed above, and further in view of Japan 08-167703, which is described as prior art in Applicant's specification, pages 2 and 3.


Circuit blocks for memory and CPU on the different chips would have been obvious as shown Applicant's figures 6 and 7, which are described as corresponding to the Japan 08-167703 reference at the last full paragraph of page 3 of Applicant's specification. Parallel processing is discussed throughout the Japanese reference, for example at [0097] - [0098]. If the signal is transferred from memory to CPU and back by parallel processing as taught, then the number of pad and bump arrangements would have to be "corresponding" somehow "to the number of bits of a memory."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (571) 272-1652.

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The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Sara W. Crane  
Primary Examiner  
Art Unit 2811